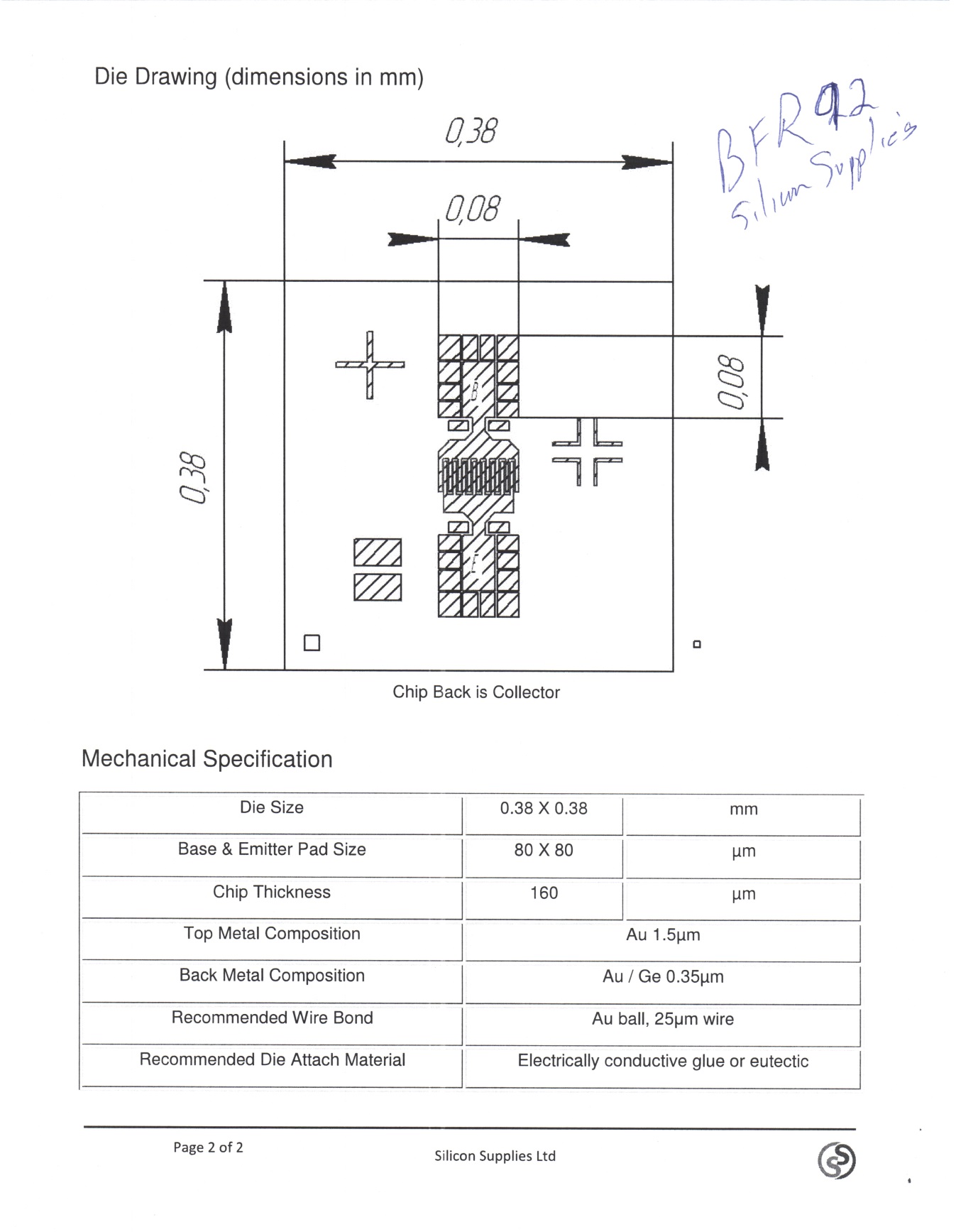
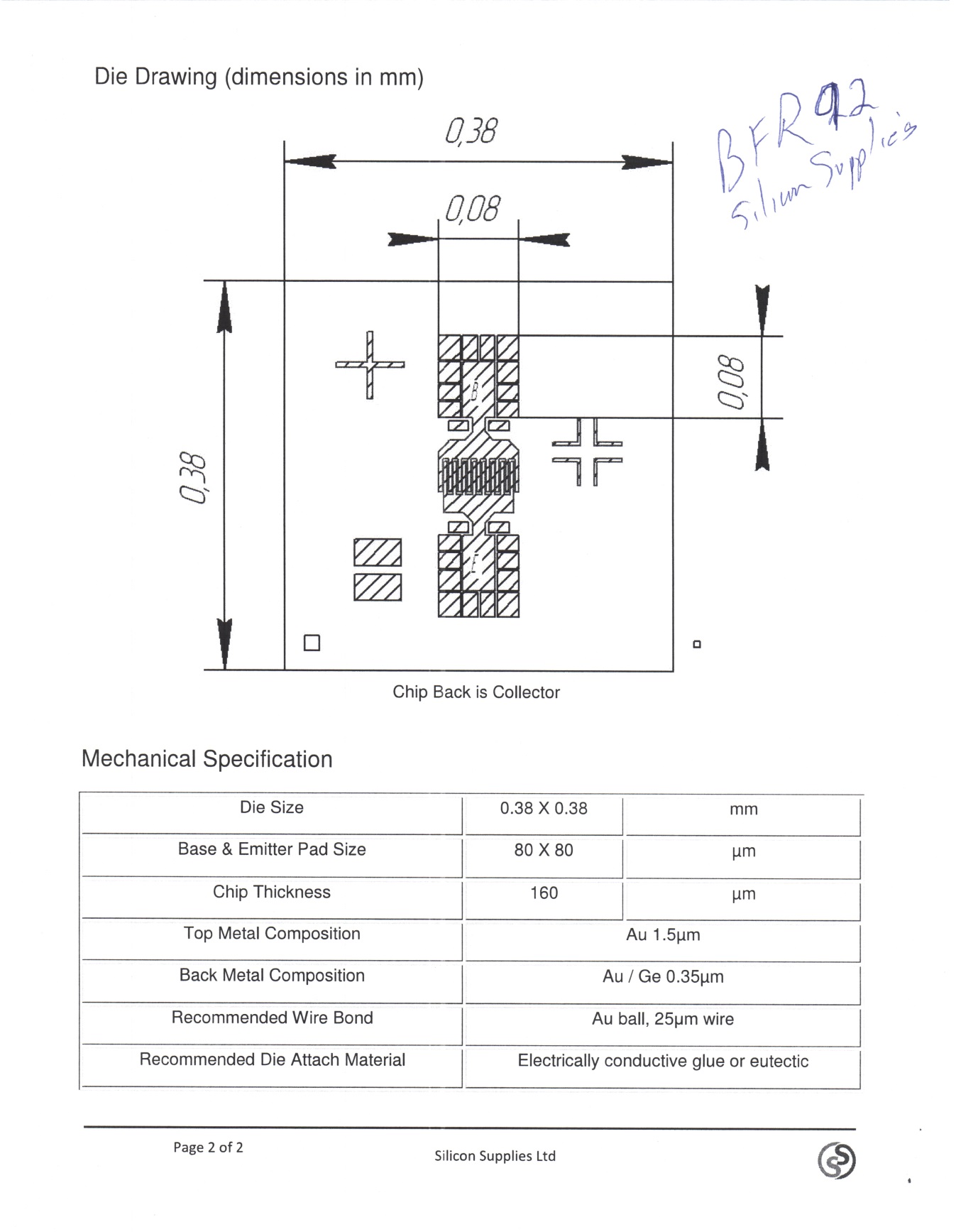
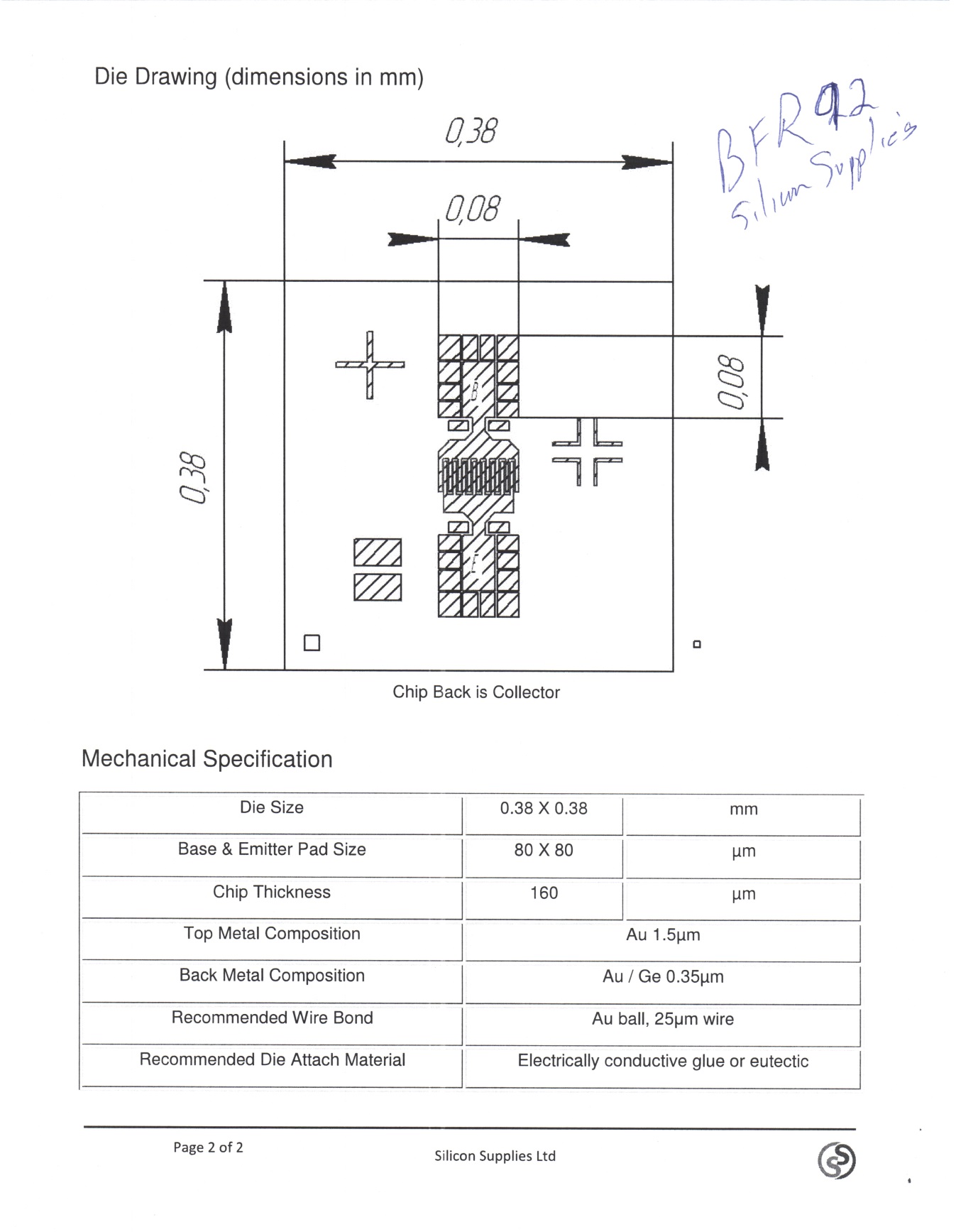
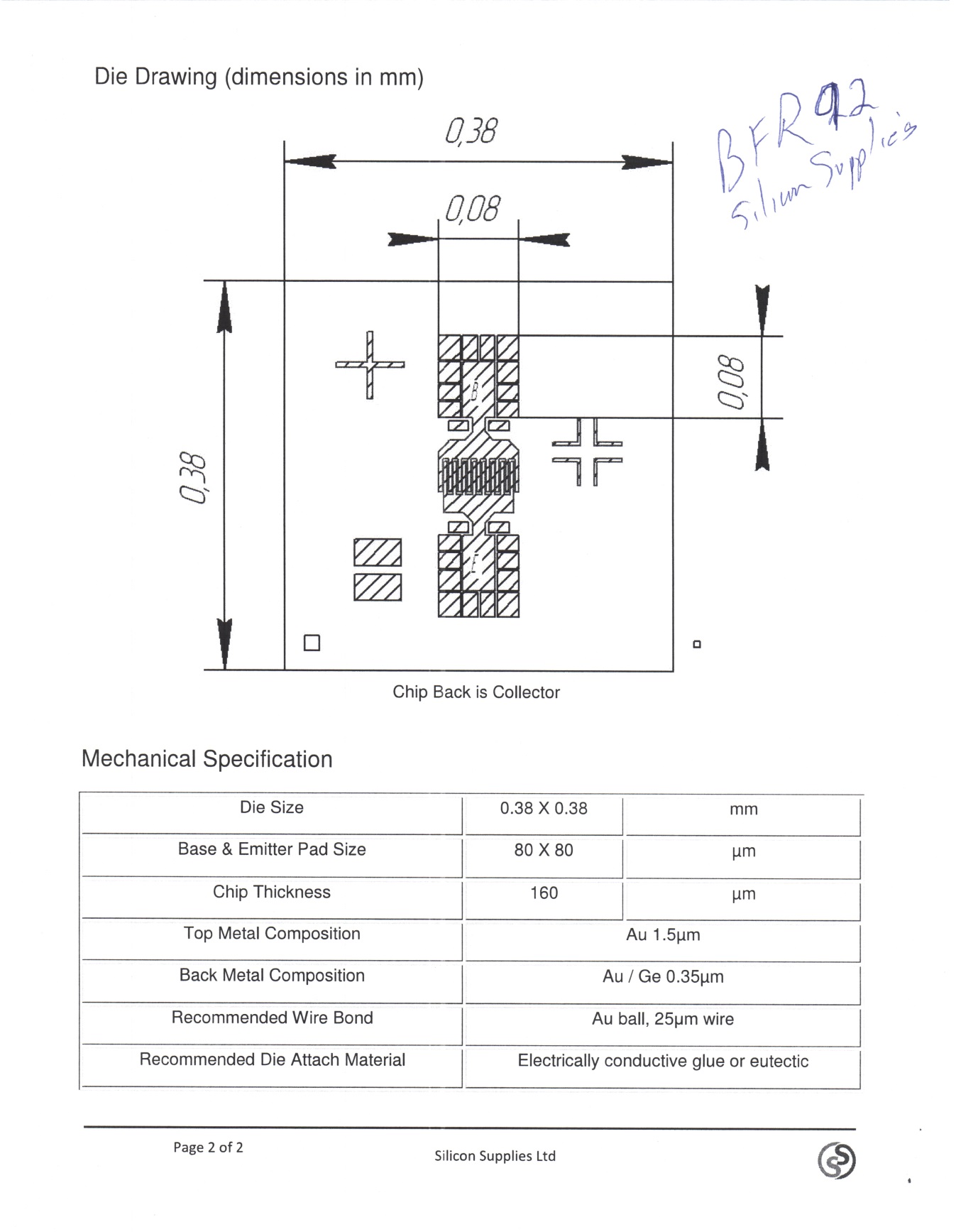
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**B**

**E**

**.015”**

**.015”**

**Top Material: Au**

**Backside Material: Au/Ge**

**Bond Pad Size: .001” X .002”**

**Backside Potential: COLLECTOR**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .015” X .015” DATE: 9/23/21**

**MFG: SILICON SUPPLIES THICKNESS .010” P/N: BFR91A**

**DG 10.1.2**

#### Rev B, 7/1